

WHAT IS CLAIMED IS:

1 1. A method of operating an electronic system having an integrated circuit
2 requiring a plurality of operating voltages comprising:
3 providing a signal from the integrated circuit to power controller circuitry;
4 decoding the signal using the power controller circuitry and generating first and
5 second control signals;
6 receiving the first control signal in a first programmable voltage generator, which
7 generates a first voltage;
8 receiving the second control signal in a second programmable voltage generator,
9 which generates a second voltage, different from the first voltage; and
10 providing the first and second voltages to the integrated circuit.

1 2. The method of claim 1 wherein the signal from the integrated circuit is in
2 the form of a string of serial binary data.

1 3. The method of claim 1 wherein the integrated circuit is a field
2 programmable gate array or programmable logic device.

1 4. The method of claim 1 herein the signal from the integrated circuit to
2 power controller circuitry is a first value to provide higher performance and a second value to
3 provide reduced power consumption.

1 5. The method of claim 1 wherein the signal from the integrated circuit to
2 power controller circuitry varies depending on environmental conditions in which the electronic
3 system is operating.

1 6. A method of operating an electronic system comprising:
2 providing a first module, having a master integrated circuit, coupled to the
3 electronic system;
4 providing a second module, having a slave integrated circuit, coupled to the
5 electronic system;
6 determining a common communication standard usable by both the master and
7 slave integrated circuits;

transferring data from the master integrated circuit to a first programmable power supply to generate voltages for to configure the master integrated circuit to use the common communication standard; and

transferring data from the slave integrated circuit to a second programmable power supply to generate voltages to configure the slave integrated circuit to use the common communication standard.

7. The method of claim 6 wherein the determining a common communication standard usable by both the master and slave integrated circuits comprises:
sending from the slave integrated circuit to the master integrated circuit a list of potential communications standards acceptable by the slave integrated circuit;
in the master integrated circuit, comparing the list of potential communications standards acceptable by the slave integrated circuit to a list of potential communications standards acceptable by the master integrated circuit;
in the master integrated circuit, selecting from the list of potential communications standards acceptable by the master and slave integrated circuits the common communication standard usable by both the master and slave integrated circuits; and
sending data from the master integrated circuit to the slave integrated circuit indicating that the common communication standard usable by both the master and slave integrated circuits should be used by the slave integrated circuit.

8. The method of claim 6 wherein the determining a common communication standard usable by both the master and slave integrated circuits comprises:
in the master integrated circuit, comparing the list of potential communications standards acceptable by the slave integrated circuit to a list of potential communications standards acceptable by the master integrated circuit, wherein the master integrated circuit varies a power control signal so as to avoid damaging the master or slave integrated circuit.

9. A method of operating an electronic system comprising:
providing a master integrated circuit coupled to the electronic system;
providing a first module, having a first slave integrated circuit, coupled to the electronic system;

5 determining a common communication standard usable by both the master and
6 first slave integrated circuits;
7 transferring data from the master integrated circuit to a first programmable power
8 supply to generate voltages for to configure the master integrated circuit to use the common
9 communication standard; and
10 transferring data from the first slave integrated circuit to a second programmable
11 power supply to generate voltages to configure the first slave integrated circuit to use the
12 common communication standard.

1 10. The method of claim 9 further comprising:
2 providing a second module, having a second slave integrated circuit, coupled to
3 the electronic system;
4 determining a common communication standard usable by both the master and
5 second slave integrated circuits;
6 transferring data from the second slave integrated circuit to a third programmable
7 power supply to generate voltages to configure the second slave integrated circuit to use the
8 common communication standard.

1 11. The method of claim 9 wherein the master integrated circuit is in a third
2 module, coupled to the electronic system.

1 12. The method of claim 9 wherein the master integrated circuit is on a
2 motherboard of the electronic system.

1 13. A method of operating an electronic system having a first integrated
2 circuit requiring a plurality of operating voltages comprising:
3 providing a signal from a second integrated circuit to power controller circuitry;
4 decoding the signal using the power controller circuitry and generating first and
5 second control signals;
6 receiving the first control signal in a first programmable voltage generator, which
7 generates a first voltage;
8 receiving the second control signal in a second programmable voltage generator,
9 which generates a second voltage, different from the first voltage; and

10 providing the first and second voltages to the first integrated circuit.

- 1 14. The method of claim 13 wherein the signal from the second integrated
2 circuit is in the form of a string of serial binary data.

1 15. The method of claim 13 wherein the second integrated circuit comprises a
2 programmable read-only memory (PROM); erasable programmable read-only memory
3 (EPROM), electrically erasable programmable read-only memory (EEPROM), serial EEPROM,
4 random access memory (RAM), dynamic random access memory (DRAM), or static random
5 access memory (SRAM).